CLAIMS

1. A processing device comprising:

a master processor;

a system memory;

a slave processor subsystem including:

a slave processor;

a shared memory accessible by said master processor and said slave processor; and

an external memory interface allowing said slave processor to access said system memory; and

a verification interface for passing system memory accesses to said system memory in a normal mode and for passing said system memory accesses to said shared memory in a verification mode.

2. The processing device of claim 1 wherein said slave processor subsystem further includes a cache memory coupled to said external memory controller and said slave processor.

3. The processing device of claim 1 wherein said verification interface includes a protocol translator for translating between a first protocol associated with memory accesses of said system memory and a second protocol associated with memory accesses of said shared memory.

4. The processing device of claim 1 wherein said verification interface comprises multiplexing circuitry for passing data to said external memory interface from either said system memory or said shared memory responsive to whether said verification interface is in a normal mode or a verification mode.

5. The processing device of claim 4 and further comprising a control interface coupled between said master processor and said shared memory.

6. The processing device of claim 5 wherein said multiplexing circuitry comprises first multiplexing circuitry and further comprising second multiplexing circuitry for passing control signals to said control interface from either said master processor or said external memory interface responsive to whether said verification interface is in a normal mode or a verification mode.

7. The processing device of claim 6 and further comprising a protocol translator for translating between a first protocol associated with memory accesses of said system memory and a second protocol associated with memory accesses of said shared memory.

8. A method of verification of a processing device including a master processor subsystem having a master processor and a system memory and a slave processor subsystem having a slave processor, a external memory interface for accessing said system memory, and a shared memory accessible by the master processor and slave processor, comprising the steps of:

passing system memory accesses to said system memory in a normal mode; and

passing system memory accesses to said shared memory in a verification mode.

9. The method of claim 8 and further comprising the step of translating between a first protocol associated with memory accesses of said system memory and a second protocol associated with memory accesses of said shared memory.

10. The processing device of claim 8 wherein said step of passing system memory accesses to said system memory comprises the step of enabling multiplexing circuitry to pass data to said external memory interface from said system memory when said verification interface is in said normal mode.

11. The processing device of claim 9 wherein said step of passing system memory accesses to said shared memory comprises the step of enabling multiplexing circuitry to pass data to said external memory interface from said shared memory when said verification interface is in said verification mode.

12. The processing device of claim 11 and further comprising a translating from a first protocol associated with memory accesses of said system memory and a second protocol associated with memory accesses of said shared memory when said verification interface is in said verification mode.

13. A processing device comprising:

a master processor;

a system memory;

a slave processor subsystem including:

one or more a slave processors;

a shared memory accessible by said master processor and said slave processor; and

an system memory interface allowing said slave processors to access said system memory; and

a verification interface for passing system memory accesses to said system memory in a normal mode and for passing said system memory accesses to said shared memory in a verification mode.

14. The processing device of claim 13 wherein said system memory interface comprises:

respective external memory interfaces associated with each slave processor; and

a memory arbiter for arbiting between memory accesses generated by each of said external memory interfaces.

15. The processing device of claim 13 wherein said slave processor subsystem further includes cache memories associated with each of said slave processors.

16. The processing device of claim 13 wherein said verification interface includes a protocol translator for translating between a first protocol associated with memory accesses of said system memory and a second protocol associated with memory accesses of said shared memory.

17. The processing device of claim 13 wherein said verification interface comprises multiplexing circuitry for passing data to said system memory interface from either said system memory or said shared memory responsive to whether said verification interface is in a normal mode or a verification mode.

18. The processing device of claim 17 and further comprising a control interface coupled between said master processor and said shared memory.

19. The processing device of claim 18 wherein said multiplexing circuitry comprises first multiplexing circuitry and further comprising second multiplexing circuitry for passing control signals to said control interface from either said master processor or said system memory interface responsive to whether said verification interface is in a normal mode or a verification mode.

20. The processing device of claim 19 and further comprising a protocol translator for translating between a first protocol associated with memory accesses of said system memory and a second protocol associated with memory accesses of said shared memory.